APPLICATION NO. 10663666

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CLMPTO

1. A method of forming semiconductor device, said method comprising the steps of:

providing a semiconductor substrate having a first conductive layer and an epi-layer doped with the same type impurities but is doped lightly than said first conductive layer;

forming a first oxide layer on said epi-layer;

forming a first photoresist pattern on said first oxide layer to define guard ring regions;

performing a first etching step etching said first oxide layer by using said first photoresist pattern as a mask;

stripping away said first photoresist pattern;

forming a polycrystalline silicon layer on all areas;

performing a blanket ion implant to implant p type impurities into said polycrystalline silicon layer;

performing an anneal process to form p regions using said doped polycrystalline silicon layer as an impurity source.

forming a second oxide layer by oxidizing said polycrystalline silicon layer and driving impurities doped said ion implant to expand said p regions thereby forming said guard ring regions;

forming a second photoresist pattern to exposed an active region;

etching said second oxide layer using said second photoresist pattern as a mask;

removing said second photoresist pattern;

forming a barrier metal layer on entire surfaces of said substrate;

performing a thermal anneal to form metal silicide layer by consuming silicon of said epi-layer;

removing unreacted barrier metal layer;

forming a top metal layer on entire surfaces;

patterning said top metal layer to define an anode electrode;

removing layers formed on a backside surface of said semiconductor substrate during forgoing steps; and

forming a backside metal layer on said backside surface, said backside metal layer acted as a cathode.

2. The method according to Claim 1 wherein said ion implant implants BF_2+ and/or boron using a dosage and energy between about 1E11 to 5E16/cm^2 and 10 to 400keV, respectively.

3. The method according to Claim 1 wherein said polycrystalline silicon layer has a thickness between about 20 to 1000 nm.

4. The method according to Claim 1 wherein said step of annealing process is performed at a temperature between about 200 to 850°C.

5. The method according to Claim 1 wherein said barrier metal layer is made of material selected from the group consisting of Ti, Ni, Cr, Mo, Pt, Zr, W and the combination thereof and wherein said top metal layer is formed of stack layers of TiNi/Ag or Al.

6. The method according to Claim 1 wherein said second photoresist pattern is partially over said guard ring regions and thus said active region is at a region between two guard ring regions and includes a portion of them.

CLAIMS 7-9 (CANCELLED)